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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,762	GILKERSON, PAUL ANTHONY	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz Fleming

Supervisory PRIMARY EXAMINER 4/1/2006

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Element number 310 of figure 4A and 4B. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because of the length. Abstracts are limited to 150 words and the submitted abstract is approximately 257 words. Correction is required. See MPEP § 608.01(b).

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Branch Prediction in a Data Processing Apparatus By Tracking Instruction Flow Changes Within a Prefetch Unit Utilizing a Return Stack."

Claim Objections

4. Claims 3-5 are objected to because of the following informalities:

Claim 3 recites the limitation "the prefetch logic" in lines 26 and 28 of page 19. There is a lack of antecedent basis for the limitations. It is suggested that the 35 U.S.C. 112 rejections below be corrected (in which case the claim objection will no longer apply).

Claims 4-5 are rejected because of their dependency on claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1- 9 are rejected under 35 U.S.C. 112.

Claim 1 recites the limitation "the prefetch logic" in lines 13-14, and 18. There is insufficient antecedent basis for this limitation in the claim. It is suggested the first limitation be changed to "a prefetch logic."

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 10 & 13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. There are no tangible end results from implementing the claims in question because the end result is a determination, which lacks a tangible "real world" result. Although some claims do have intermediate steps that produce an intermediate tangible result, the end result is merely a determination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by McMahan (U.S. Patent # 5,692,168), herein referred to as McMahan.

As per claim 1, McMahan discloses a data processing apparatus, comprising:

a processor operable to execute instructions (CPU core 20, see figure 1a: There are also two separate components for execution (EX_X 23X and EX_Y 23Y));

a prefetch unit (Prefetcher 35, see figure 1a) operable to prefetch instructions from a memory (See column 13, lines 23-25: the instructions are fetched from cache) prior to sending those instructions to the processor for execution (See figure 3b: The prefetch stage 179 is taken before the execution/write-back stage 180), the prefetch unit being operable to determine for a prefetched instruction whether that prefetched instruction is an instruction flow changing instruction (See column 22, lines 25-31: The flow control logic determines if instruction flow has changed is associated with the prefetch buffer), and based thereon to determine a fetch address for a next instruction to be prefetched by the prefetch unit (See column 22, lines 32-36: The flow control logic predicts what the change of flow address could be as well as has the target address available);

a return stack accessible by the prefetch unit (See figure 1a and 5a: The branch prediction unit 40, which houses the stack, is coupled to the prefetcher 35) and operable to hold one or more addresses (See column 31, lines 3: The stack can hold 8 addresses); and

prediction logic operable (See figure 4f: The flow control logic performs predictions), if the prefetched instruction is a conditional instruction, to predict whether that prefetched instruction will be executed by the processor (See column 22, lines 37-41: A predicted change of flow address is available), the

prefetch logic being operable to determine the fetch address dependent on the prediction from the prediction logic (See column 22, lines 37-41: The flow control logic determines both a target address and a change of flow address);

in the event that the prefetched instruction is a first type of instruction flow changing instruction and is conditional, and the prediction logic predicts that that prefetched instruction will be executed, the prefetch logic being operable to determine as the fetch address an address obtained from the return stack (See column 31, lines 42-47: Prefetcher gets an address from the return stack).

As per claim 2, McMahan discloses wherein the first type of instruction flow changing instruction is a procedure return instruction operable when executed to cause the processor to return from a procedure being executed by the processor (See column 7, lines 53-61: Information regarding what data/instruction is in each stage of the pipeline is saved or stalled when a squash or interrupt is found).

As per claim 3, McMahan discloses wherein if the prefetch logic determines that the prefetched instruction is a second type of instruction flow changing instruction (See column 12, lines 28-31: There are 2 types of flow changes), the prefetch logic is further operable to determine a return address (See column 31, lines 21-27: A return address is known and stored in the stack) and to cause that return address to be placed on the return stack (See column 31, lines 21-27: A return address is stored in the stack).

As per claim 4, McMahan discloses wherein said second type of instruction flow changing instruction is a branch with link instruction (See column 12, lines 28-31: Branches are 1 of 2 types of flow changes), which is operable to identify a start address for a procedure to be executed by the processor (See column 12, lines 42-44: A predicted branch supplies a target address), upon returning from the procedure the next instruction to be executed by the processor being specified by the return address (See column 31, lines 21-27: A return address is stored in the stack).

As per claim 5, McMahan discloses wherein the procedure is returned from by execution of one of said first type of instruction flow changing instructions (See column 31, lines 3-12: A return address is popped off the stack when a return this in the target cache).

As per claim 6, McMahan discloses wherein said prediction logic is a dynamic prediction logic which is operable to provide a prediction as to whether the prefetched instruction will be executed by the processor dependent upon history information identifying an outcome of conditional instructions previously executed by the processor (See column 12, lines 32-26: History is used in branch prediction).

As per claim 7, McMahan discloses wherein said prediction logic is provided within said prefetch unit (See figure 3a: The branch prediction unit 40 is part of the prefetch unit).

As per claim 8, McMahan discloses wherein said return stack is provided within said prefetch unit (See figure 3a: The return stack 130 is a part of the BPU 40).

As per claim 9, McMahan discloses wherein said prefetch unit comprises decode logic operable to determine for the prefetched instruction whether that prefetched instruction is an instruction flow changing instruction (See column 22, lines 43- 49: A bit is set for flow changes), and control logic operable in response to the decode logic to determine the fetch address for the next instruction to be prefetched by the prefetch unit (See column 22, lines 37-41 and 50-53: The instructions are decoded accordingly to flow change bit and the flow control logic determines both a target address and a change of flow address).

As per claim 10, McMahan discloses a method of operating a data processing apparatus comprising a processor operable to execute instructions (CPU core 20, see figure 1a: There are also two separate components for execution (EX_X 23X and EX_Y 23Y)), a prefetch unit (Prefetcher 35, see figure 1a) operable to prefetch instructions from a memory (See column 13, lines 23-25: the instructions are fetched from cache) prior to sending those instructions to the

processor for execution (See figure 3b: The prefetch stage 179 is taken before the execution/write-back stage 180), and a return stack accessible by the prefetch unit (See figure 1a and 5a: The branch prediction unit 40, which houses the stack, is coupled to the prefetcher 35) and operable to hold one or more addresses (See column 31, lines 3: The stack can hold 8 addresses), the method comprising the steps of:

(a) determining for a prefetched instruction whether that prefetched instruction is an instruction flow changing instruction (See column 22, lines 25-31: The flow control logic determines if instruction flow has changed is associated with the prefetch buffer), and based thereon determining a fetch address for a next instruction to be prefetched by the prefetch unit (See column 22, lines 32-36: The flow control logic predicts what the change of flow address could be as well as has the target address available);

(b) if the prefetched instruction is a conditional instruction, predicting whether that prefetched instruction will be executed by the processor (See column 22, lines 37-41: A predicted change of flow address is available), and at said step (a) determining the fetch address dependent on the prediction (See column 22, lines 37-41: The flow control logic determines both a target address and a change of flow address); and

(c) in the event that the prefetched instruction is a first type of instruction flow changing instruction and is conditional, and if said step (b) predicts that that prefetched instruction will be executed, determining as the fetch address an

address obtained from the return stack (See column 31, lines 42-47: Prefetcher gets an address from the return stack).

As per claim 11, McMahan discloses wherein the first type of instruction flow changing instruction is a procedure return instruction operable when executed to cause the processor to return from a procedure being executed by the processor (See column 7, lines 53-61: Information regarding what data/instruction is in each stage of the pipeline is saved or stalled when a squash or interrupt is found).

As per claim 12, McMahan discloses wherein if at said step (a) it is determined that the prefetched instruction is a second type of instruction flow changing instruction (See column 12, lines 28-31: There are 2 types of flow changes), the method further comprises the steps of:

determining a return address (See column 31, lines 21-27: A return address is known and stored in the stack); and

placing that return address on the return stack (See column 31, lines 21-27: A return address is stored in the stack).

As per claim 13, McMahan discloses wherein said second type of instruction flow changing instruction is a branch with link instruction (See column 12, lines 28-31: Branches are 1 of 2 types of flow changes), which is operable to identify a start address for a procedure to be executed by the processor (See

column 12, lines 42-44: A predicted branch supplies a target address), upon returning from the procedure the next instruction to be executed by the processor being specified by the return address (See column 31, lines 21-27: A return address is stored in the stack).

As per claim 14, McMahan discloses further comprising the step of returning from the procedure by execution of one of said first type of instruction flow changing instructions (See column 31, lines 3-12: A return address is popped off the stack when a return this in the target cache).

As per claim 15, McMahan discloses wherein said step (b) comprises the step of providing a prediction as to whether the prefetched instruction will be executed by the processor dependent upon history information identifying an outcome of conditional instructions previously executed by the processor (See column 12, lines 32-26: History is used in branch prediction).

As per claim 16, McMahan discloses wherein said step (b) is performed within said prefetch unit (See figure 3a: The branch prediction unit 40 is part of the prefetch unit).

As per claim 17, McMahan discloses wherein said return stack is provided within said prefetch unit (See figure 3a: The return stack 130 is a part of the BPU 40).

As per claim 18, McMahan discloses wherein said prefetch unit comprises decode logic operable to determine for the prefetched instruction whether that prefetched instruction is an instruction flow changing instruction (See column 22, lines 43- 49: A bit is set for flow changes), and control logic operable in response to the decode logic to determine the fetch address for the next instruction to be prefetched by the prefetch unit (See column 22, lines 37-41 and 50-53: The instructions are decoded accordingly to flow change bit and the flow control logic determines both a target address and a change of flow address).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to show further art related to branch prediction in a data processing apparatus by tracking instruction flow changes within a prefetch unit utilizing a return stack:

U.S. Patent # 6,035,118 to Lauterbach et al shows a mechanism to eliminate the performance penalty of computed jump targets in a pipelined processor.

U.S. Patent # 6,101,585 to Pickett et al shows fetching instructions from an instruction cache using sequential way predication.

U.S. Patent # 6,427,206 B1 to Yeh et al shows an optimized branch predication for strongly predicted compiler branches.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

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March 28, 2006

Supervisory
FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
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4/1/2006